


LCFC NM-C952

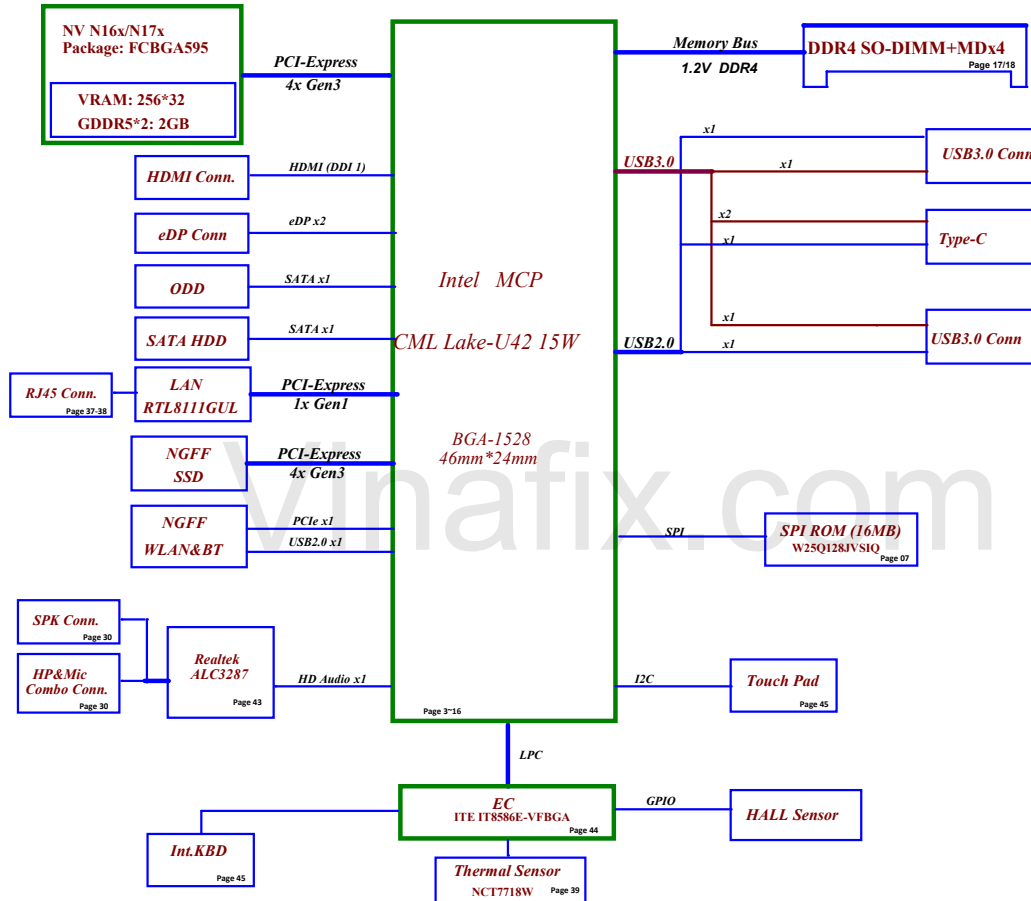
GS55C MB Schematics Document

CML U42 with DDR4 + Nvidia N16S-GTR/N17S-G3

2019-08

REV: 0.1

Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		Cover Page	
2019/07/20		2020/07/20			
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<small>Date: Wednesday, November 20, 2019 18:00</small>				<small>Rev 0.1</small>	



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane				
State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTB +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn Right
	2 USB3.0 Conn Left
	3 NC
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn Left
	2 NC
	3 USB3.0 Conn Right
	4 Finger Print
	5 Card reader
	6 NC
PCIE	7 Camera
	8 NC
	9 NC
	10 Bluetooth
	5-8 X4 DGPU
	9 Giga LAN
	10 NC
	11 SATA HDD
	12 WLAN
	13-16 X4 PCIE/GATA SSD

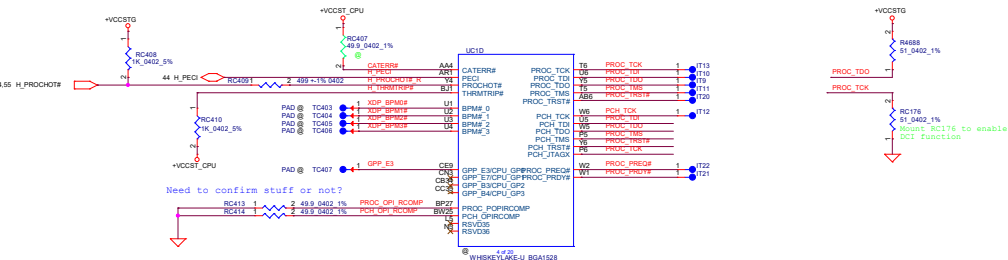
BOM Structure	BTO Item
8	Un-stuff
148	For 14" part
158	For 15" part
YOGA8	For YogaS30 part
5308	For S308 part
CDC8	For C cost down
EMC8	For EMC part
EMC 158	For EMC 15" part
EMC NS8	For EMC un-stuff part
EMC PX8	For EMC PX part
EMC_PXNS8	For EMC PX ns-stuff part
ME8	For ME part
OPT8	For NV GPU part
OPTN168	For NV H16S-GTR GPU part
OPTN178	For NV H17S-G1 GPU part
TS8	For touch screen part
TP8	For Touch Pad Part
UMA8	For UMA part

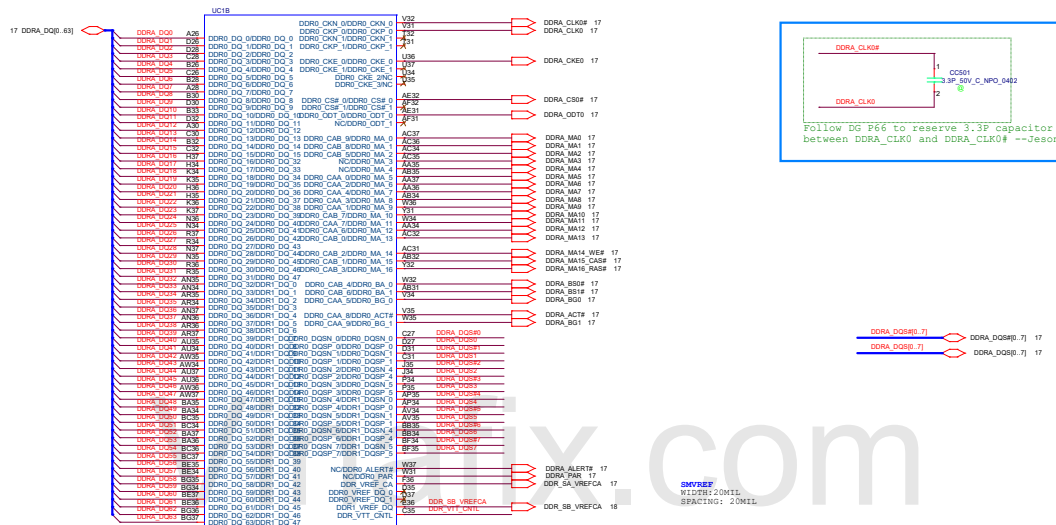
SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory	PCH	PMIC	SODIMM	Thermal	WLAN
EC_SMB_CLK1	IT8586E	V	V	X	V	X	X	X	X	X	X
EC_SMB_DA1	+3VL_EC				+3VL_EC						
EC_SMB_CLK2	IT8586E	X	X	V	V	X	V	X	X	V	X
EC_SMB_DA2	+3VS			+3VL_AGN	+3VS		+3VALW_PCH				
EC_SMB_CLK3	IT8586E	X	X	X	V	X	X	V	X	X	X
EC_SMB_DA3	+3VL_EC				+3VL_EC						
PCH_SMB_CLK	PCH	X	X	X	X	X	V	X	V	X	V
PCH_SMB_DA3A	+3VALW_PCH						+3VALW_PCH		+3VS		+3VS


EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	PMIC	need to update	DOR4 SODIMM	need to update
Charger	0001 0010 b	PCH	need to update			Wlan	Reserved
		DGPU	need to update				

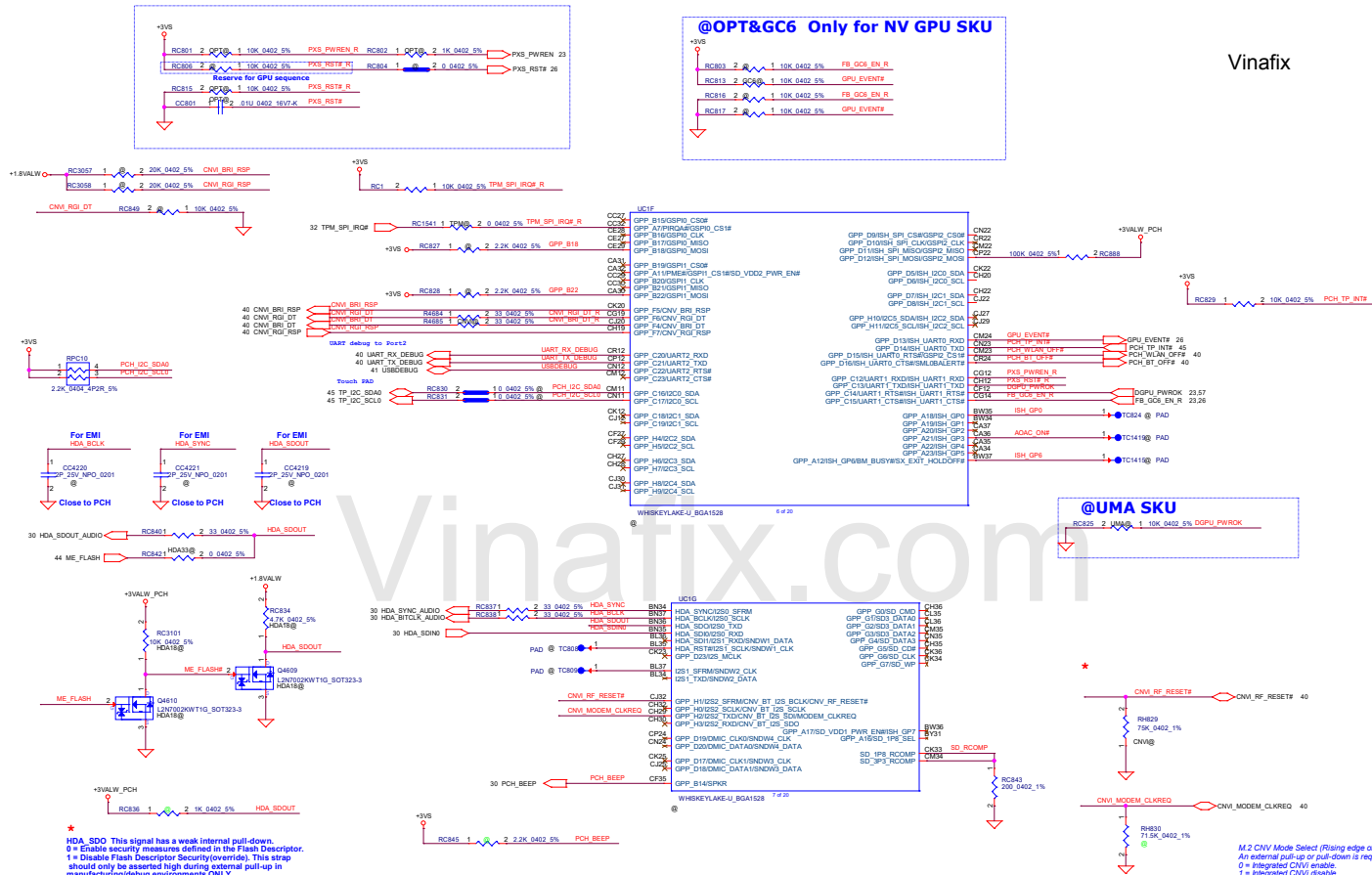






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Issued Date	2019/07/20	Deciphered Date	2020/07/20	MCP (DDR4)	
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				Size Document Number G855C	New <input type="checkbox"/>
				Information Management ID: [Blank] Sheet: 6 of 6	

@OPT&GC6 Only for NV GPU SKU







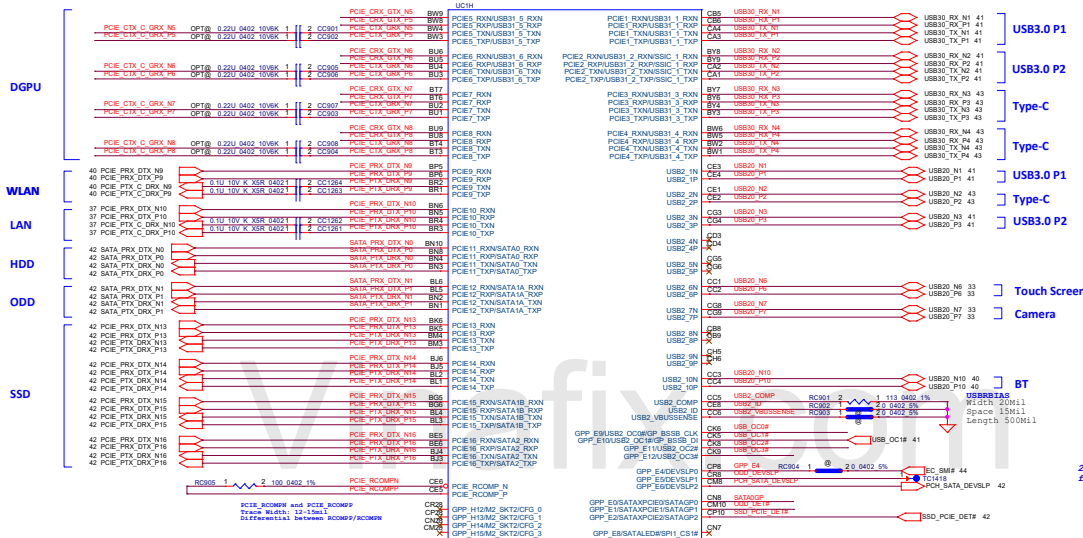
Note: Cnvi RGI_DT pin gets the pull-down resistor (1K ohm) from the internal CRF module when CNVI is enabled. There must not be any pull-down resistor connected on the board.

Pin Name	Strap Description	Configuration	Default Value	When Sampled
BPFR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) ★ 1 = Enable "Top Swap" mode	0	Rising edge of PCH_PWRON
RTT10 MOD0/ GPP_B18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) ★ 1 = Enable "No Reboot" mode	0	Rising edge of PCH_PWRON
BSPT1 MOD0/ GPP_B22	Reboot BIOS Strap Bit 0	Internal PD 0 = SPI (Default) ★	0	Rising edge of PCH_PWRON

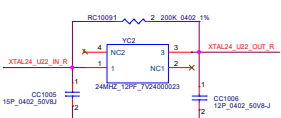
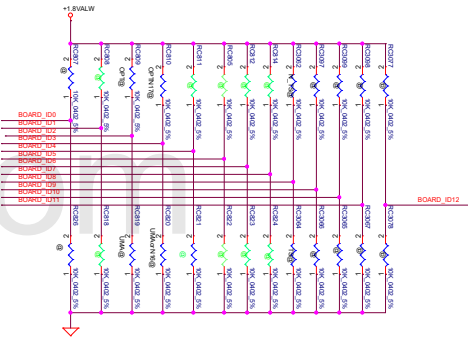
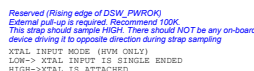
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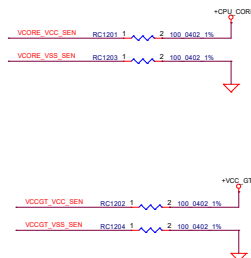
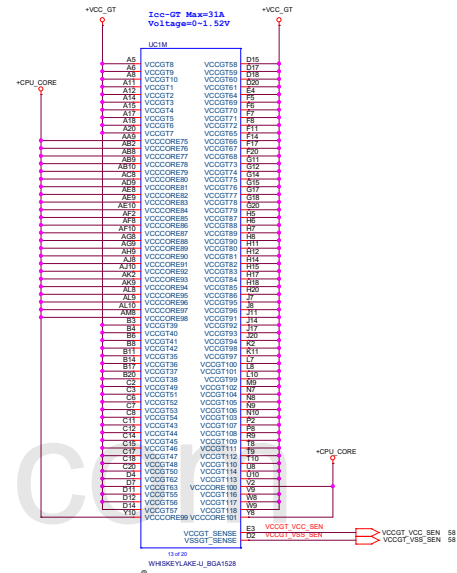
★ GPP_B18 NO REBOOT
0 = Disable "No Reboot" mode (Default)
1 = Enable "No Reboot" mode (PCH will disable the TOS)
Timer system reboot feature. This function is useful when running I/O ROM.

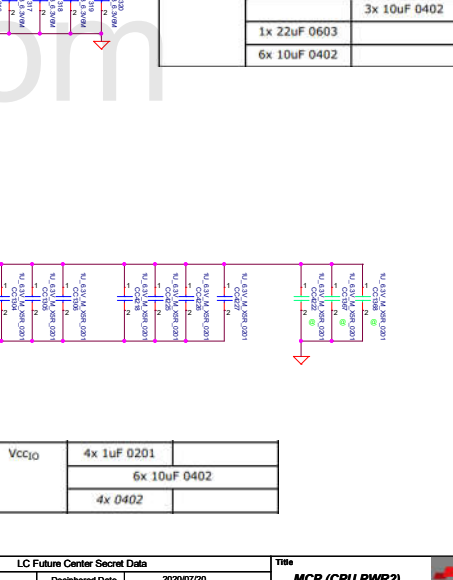
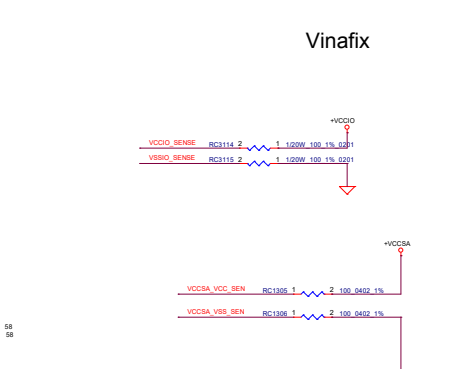
20 PCIe_CRX_GTX_N6.B] 
 20 PCIe_CRX_GTX_P6.B] 
 20 PCIe_CTX_C_GTX_N6.B] 
 20 PCIe_CTX_C_GTX_P6.B] 

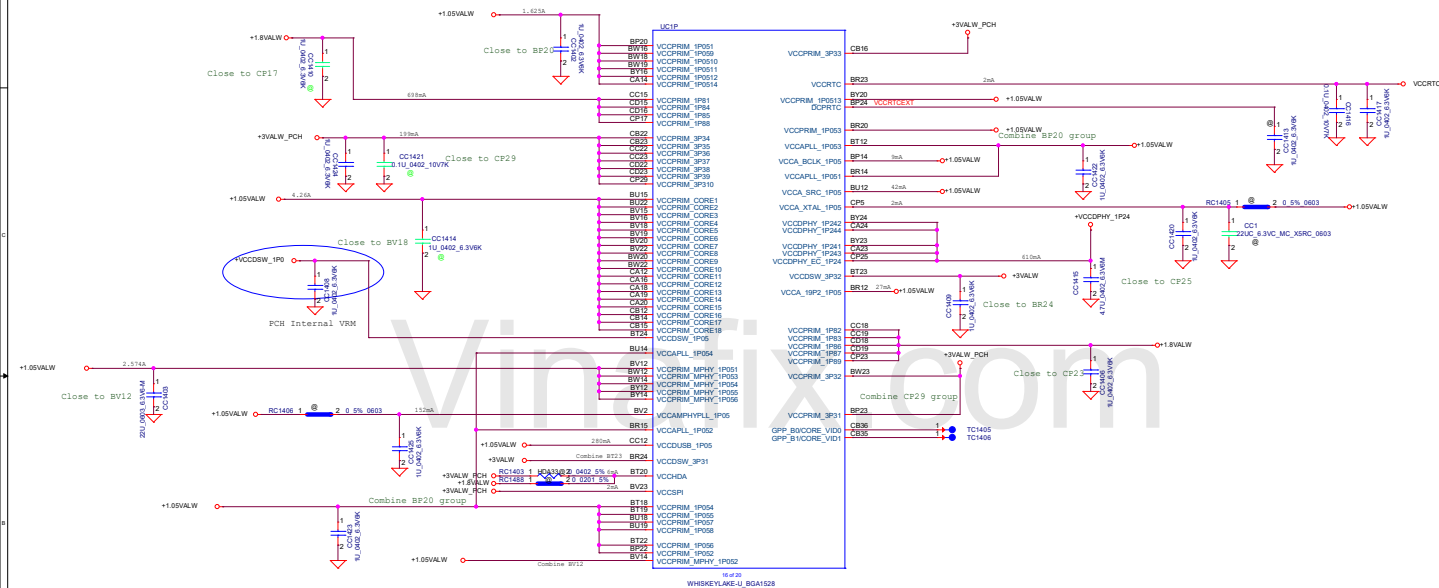


2016/05/03: Implement as Power Button
function for Windows RedStone support

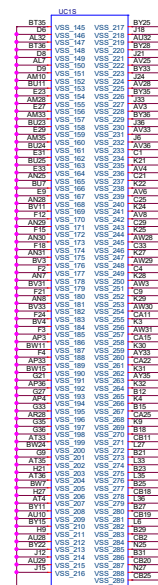




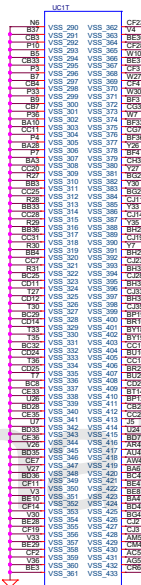




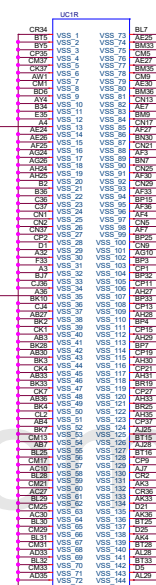
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			GSS5C
		Date:	Wednesday, November 20, 2019 14 of 01



10-02-20
 WHEREKEYLAKE-U_BGA1528




10-02-20
 WHEREKEYLAKE-U_BGA1528



10-02-20
 WHEREKEYLAKE-U_BGA1528

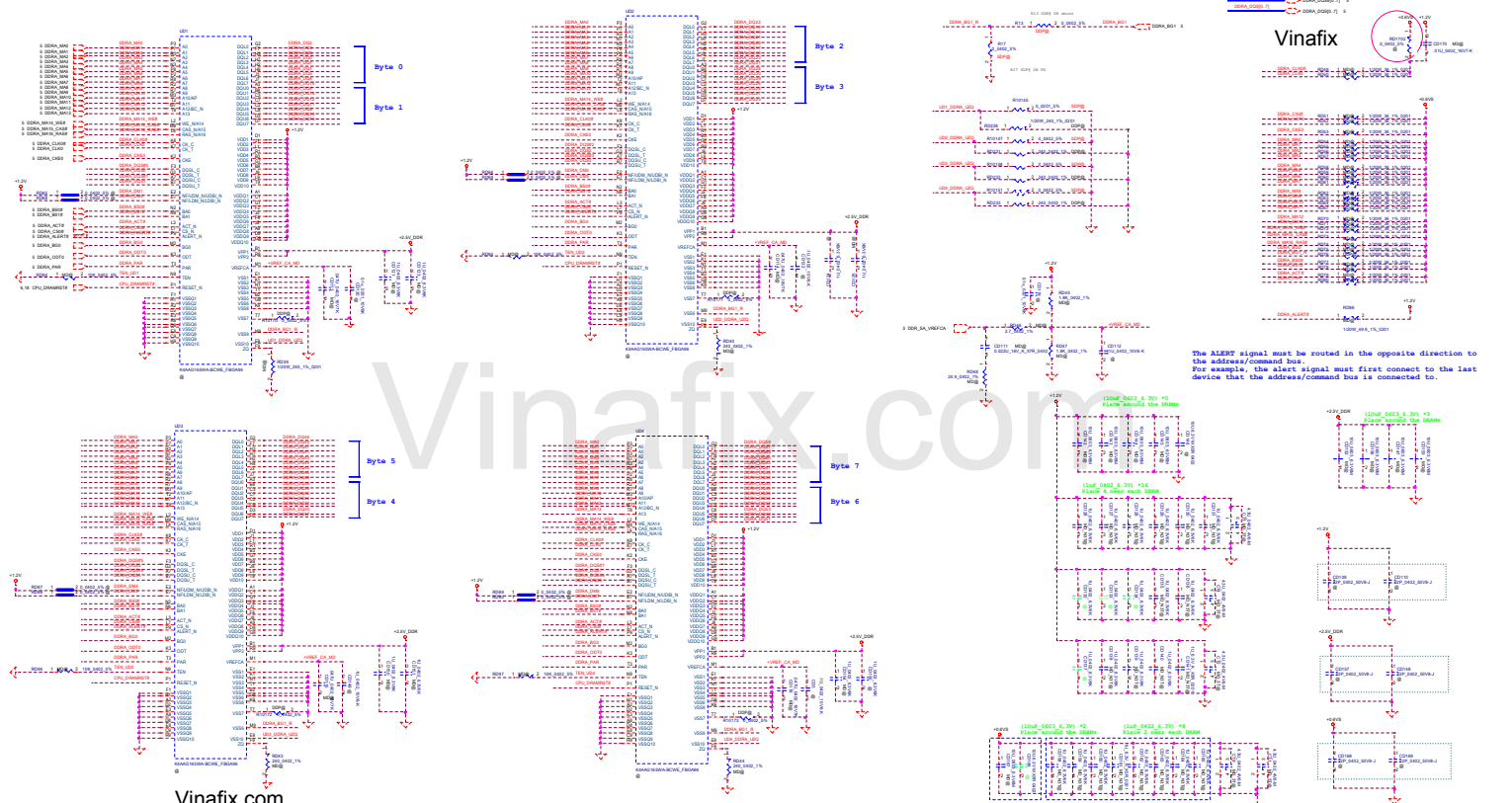
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Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		XDP	
2019/07/20		2020/07/20		XDP	
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Size				Document Number	
G855C				G855C	
Date				Wednesday, November 20, 2019	
Sheet				18 of 81	

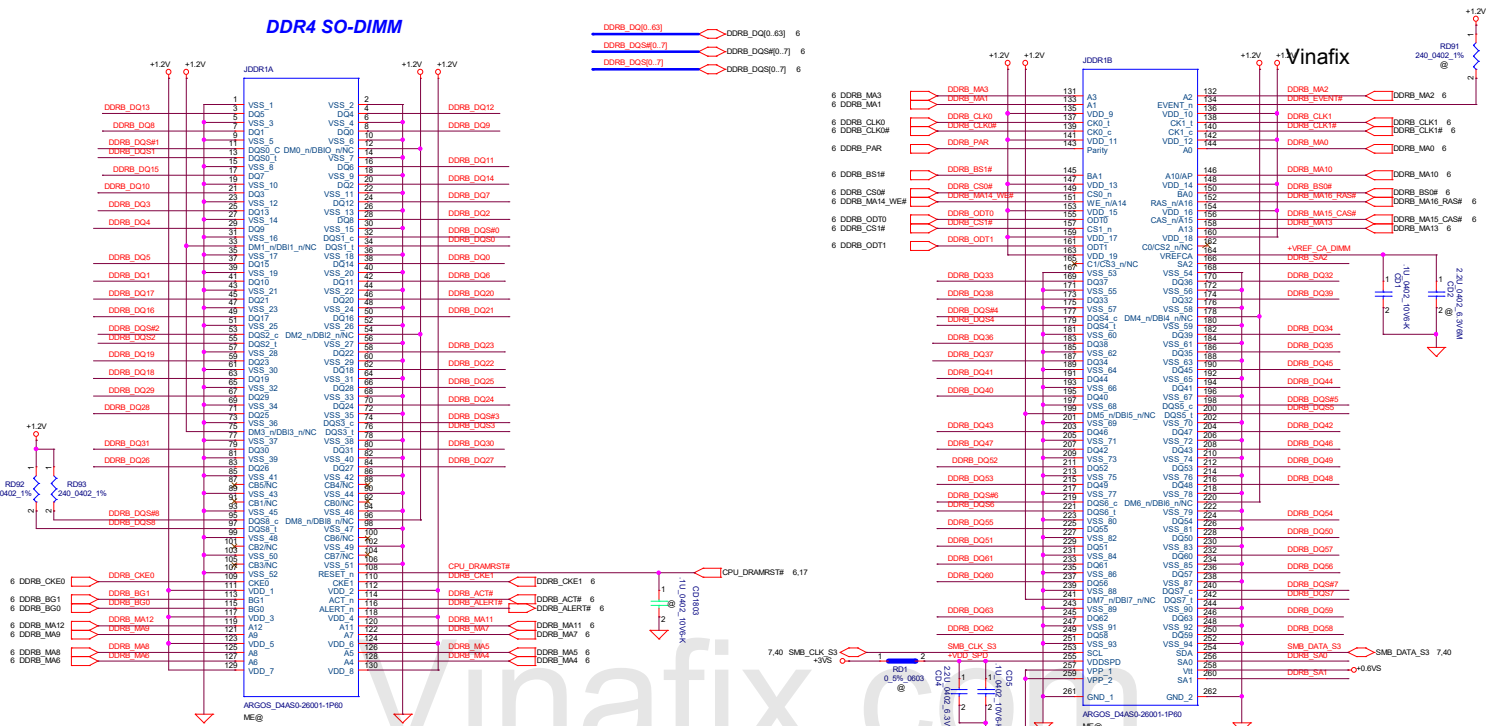


Rev
0.1

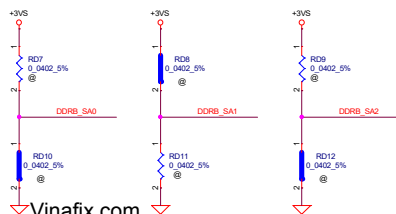
Apply X76 BOM to control DDP Memory Down stuff components!



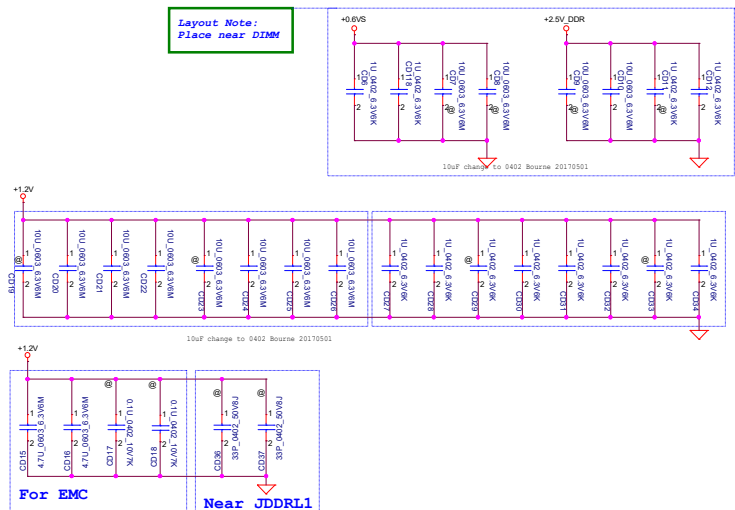
DDR4 SO-DIMM




Need to confirm SPD address setting



SPD Address = 0XA4 (follow CRB)

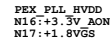
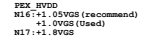
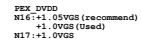
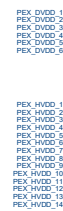
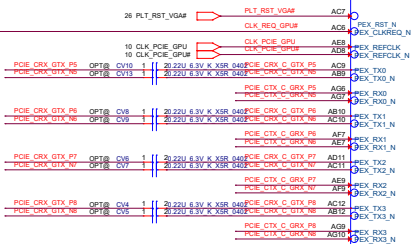


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Rev	001	Modification Number	GS55C		Rev		0.1
Date	Manufacture Month		2020/07/20		Page		01

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10k pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

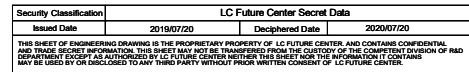
	GPU	Mem	Min Core Clk	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		(1.05V) (6)	Other (3.3V)		
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

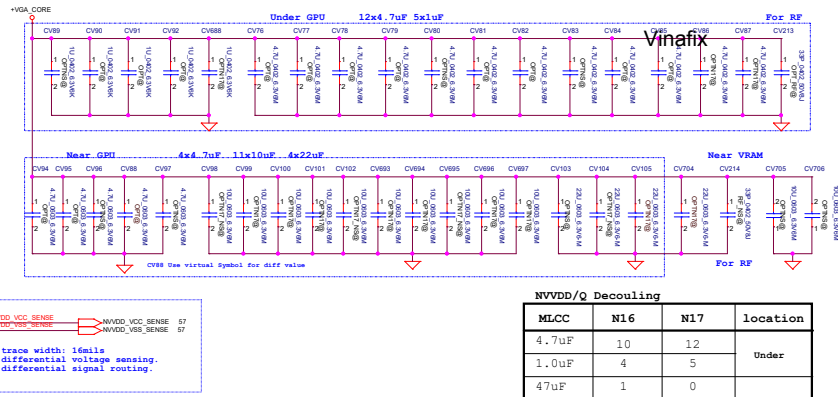
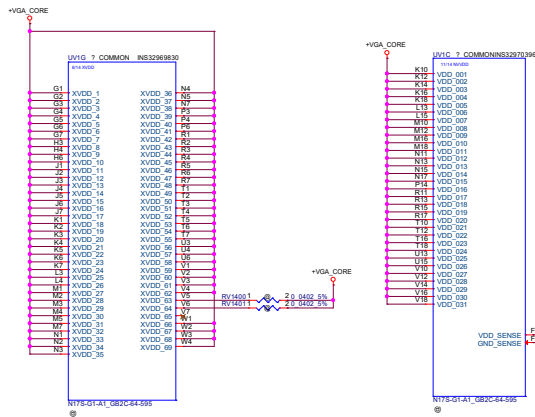
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_01	+VSS	BOOT_FROGSD	BOOT_FROGSD	BOOT_FROGSD	BOOT_FROGSD
ROM_81	+VSS	RAM_CFG[3]	RAM_CFG[1]	RAM_CFG[1]	RAM_CFG[0]
ROM_80	+VSS	PCIE_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+VSS	Reserved(keep pull-up and pull-down footprint and stuff 50kOhm pull-up)			
STRAP1	+VSS				
STRAP2	+VSS				
STRAP3	+VSS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP4	+VSS				



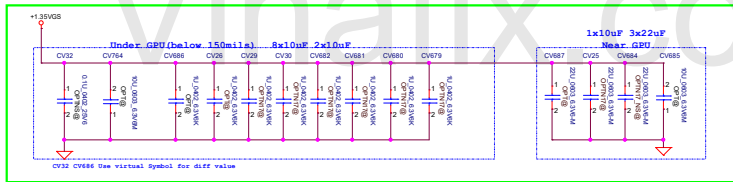
MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

MLCC	N16	N17	location
0.1uF	1	1	Near





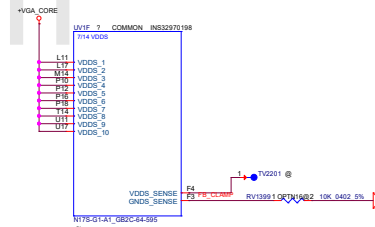
MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	
10uF	0	11	Near
22uF	1	4	
4.7uF	5	4	
330uF	1	2	



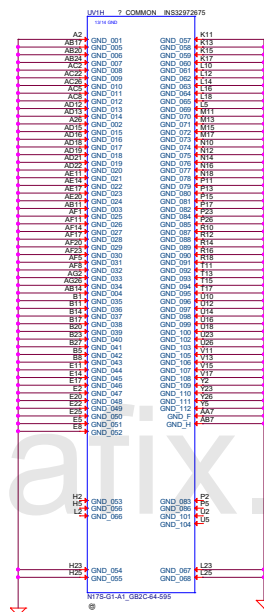
MLCC	N16	N17	location
0.1uF	2	0	
1.0uF	2	8	
4.7uF	2	0	Under
10uF	0	2	
10uF	1	1	
22uF	1	3	Near



CALIBRATION PIN	GDDR5
FB_CAL_X_PD_VDDQ	40.2Ohm
FB_CAL_X_PU_GND	40.2Ohm
FB_CAL_XTERM_GND	60.4Ohm



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MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	



MLCC	N16	N17	location
4.7uF	2	NA	Near



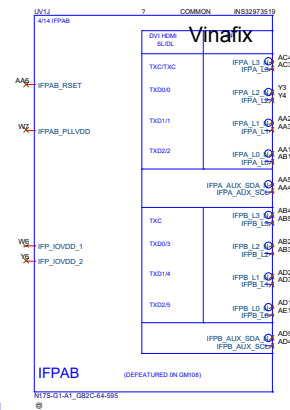
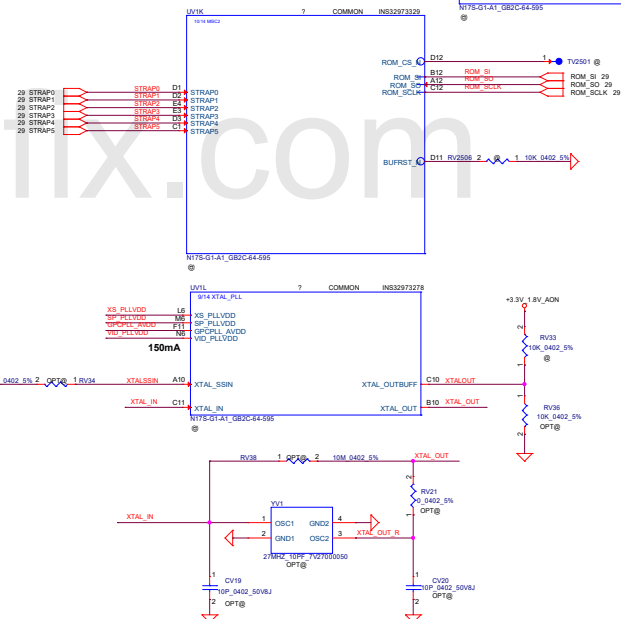
MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

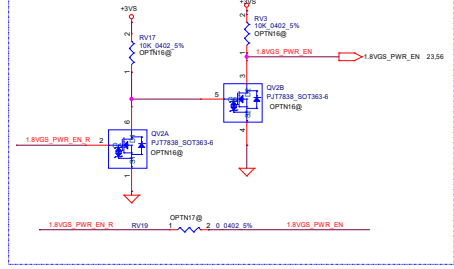
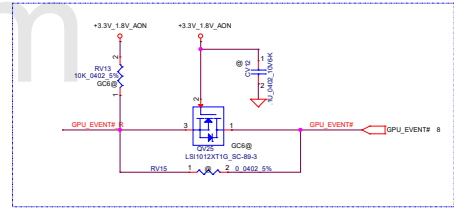
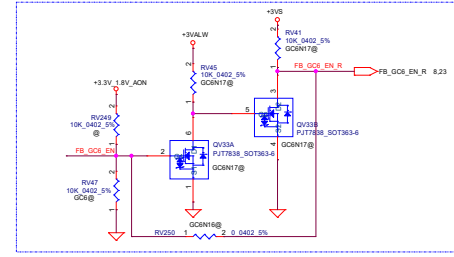
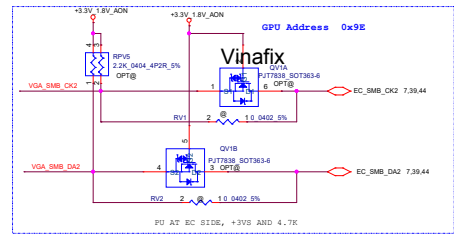
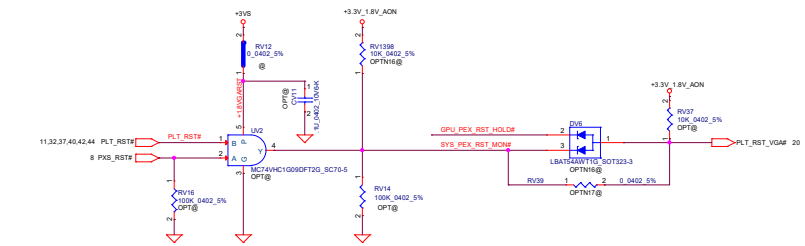
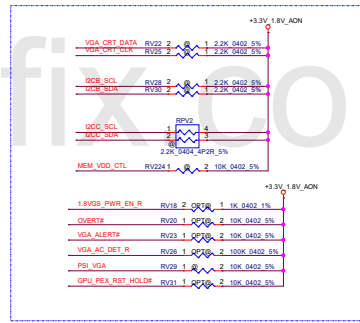
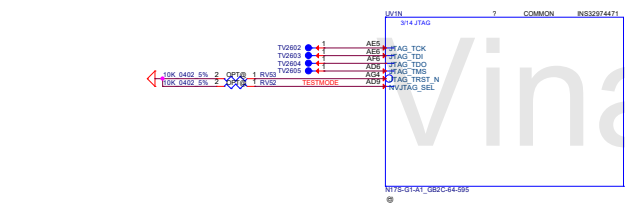
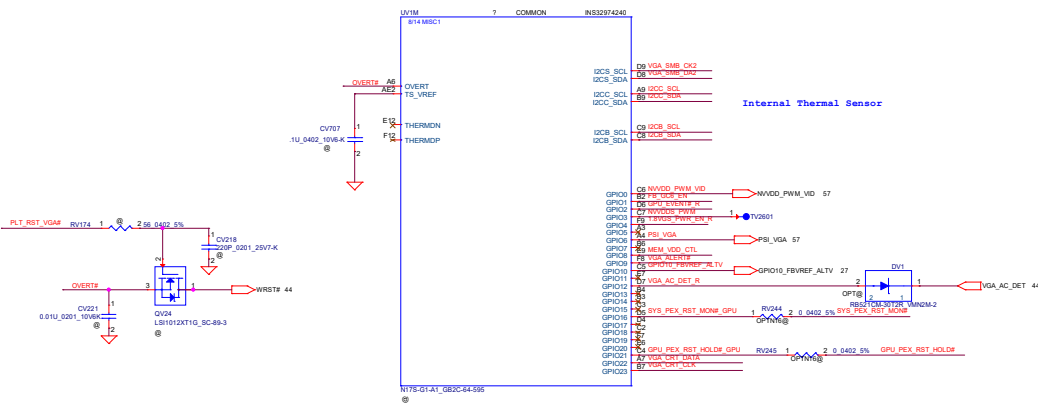


MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	



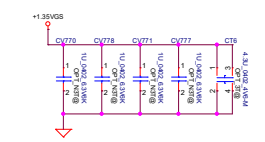
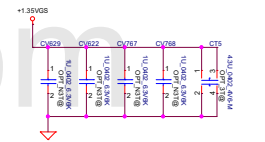
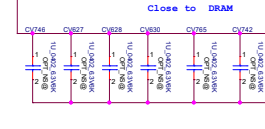
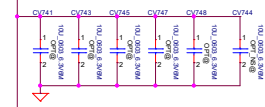
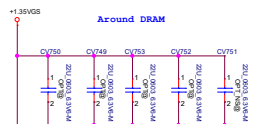
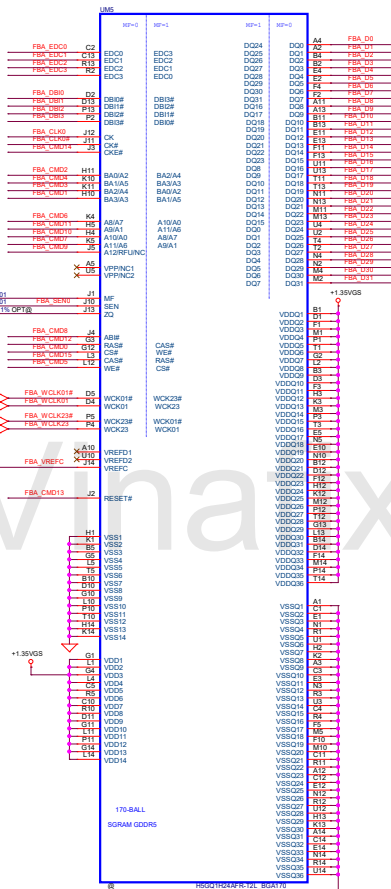
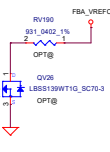
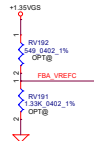
MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	





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MF=0 No Mirror

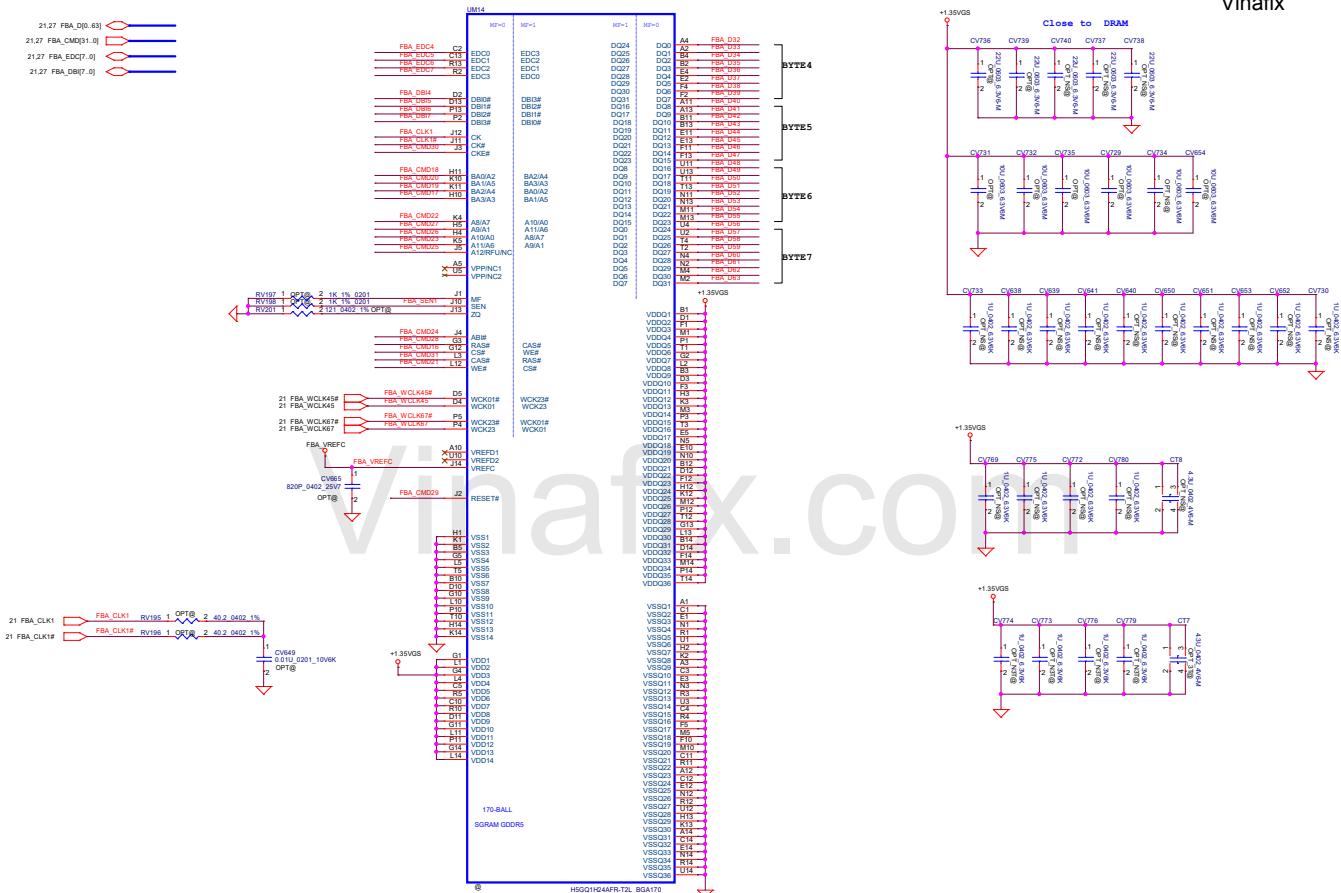


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upper 32 bits

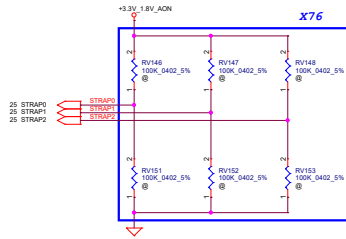
MF=0 No Mirror

Vinafix



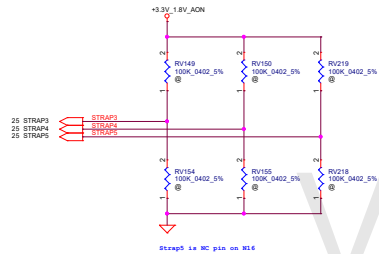
Vinafix.com

Security Classification	LC Future Center Secret Data		Title	GPU_GDDR5_Rank0 [64] LCFC	
Issued Date	2019/07/20	Deciphered Date	2020/07/20	Docu	
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				Size	Document Number
				Rev	
				G55C	
				Date:	Wednesday, November 28, 2018 11:00 AM
				28 of 01	



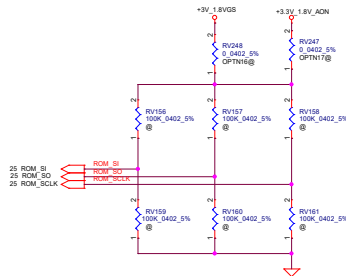
GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samseung 2Gb	K4G80325FC-BC25	0 (0x0000)	L	L	L
	Micron 2Gb	MT51J256M32HF-80	1 (0x0001)	L	L	H
	Hynix 2Gb	H5GC8H24AJR-R2C	2 (0x0010)	L	H	L

Vinafix



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE
1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGINAL
1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER
1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N179-G1	H	H	M	0000
N169-GTR				

1: ENABLE 0: DISABLE
SOR0/1/2/3 DISABLE

DEVID_SEL
0 (Default)
1

PCIE_CFG
0 (Default)
1

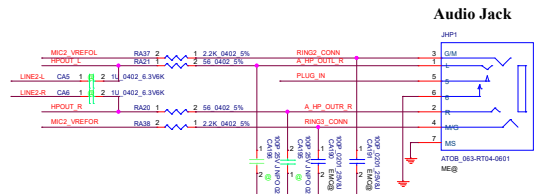
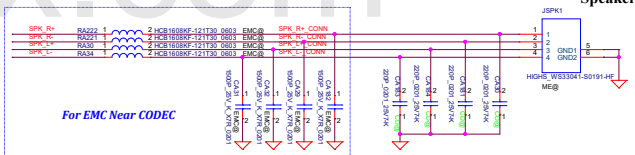
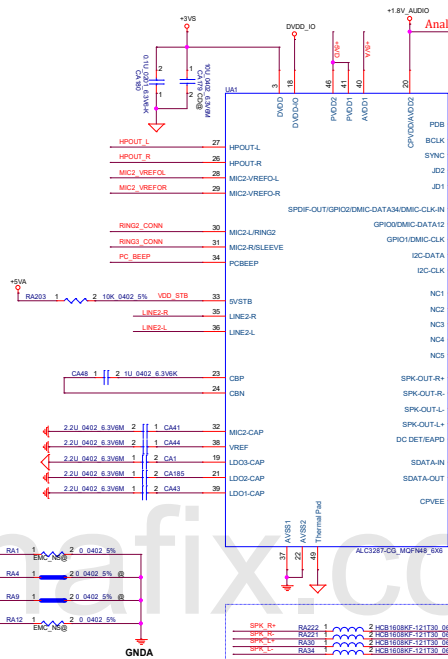
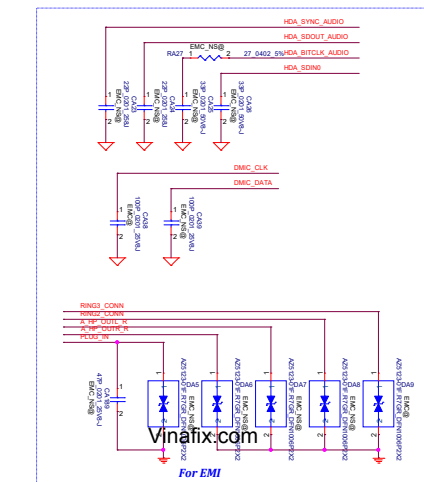
SMBUS_ALT_ADDR
0 0x9E (Default)
1 0x9C (Multi-GPU usage)

VGA_DEVICE
0 3D Device (Class Code 302h)
1 VGA Device (Default)

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Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/20	Deciphered Date	2020/07/20
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Size	Document Number	0.1
Date	Wednesday, November 20, 2019 18:58	29 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/20	Deciphered Date	2020/07/20

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Title	Codec ALC3287
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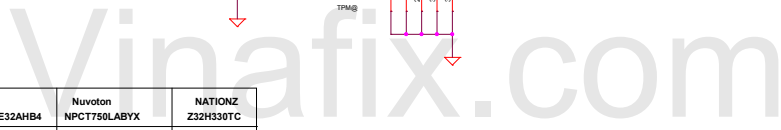
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DocId: 34600000



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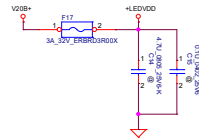
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Issued Date		Deciphered Date		Codex ALC3287	
2019/07/20		2020/07/20			
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Size				Document Number	
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Date				Wednesday, November 20, 2019 18:00	
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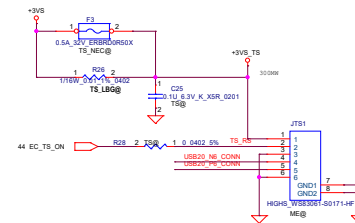
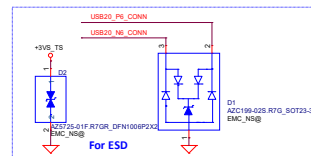
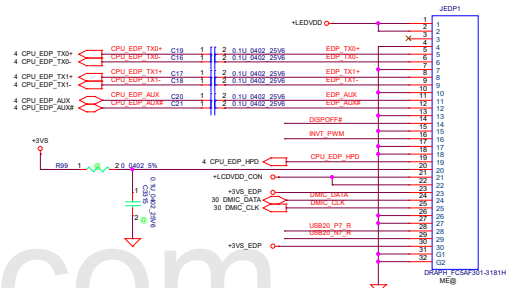
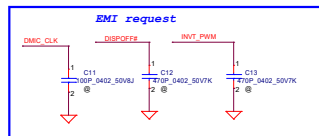
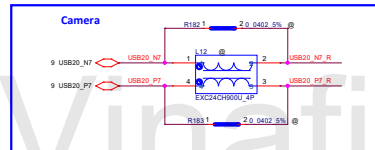
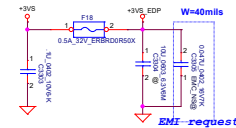
Pin No	TCG PTP Spec (v38)	Infinion SLB9670VQ2.0 FW 7.61	ST Micro ST3TH1PH2E32AHB4	Nuvoton NPCT750LABYX	NATIONZ Z32H333TC
1	VDD	NC/VDD	NC	VSB	VDD
2	GND	GND	GND	NC	GND
3	GPIO	NC	NC	NC	NC
4	GPIO	NC	NC	PP/GPIO6	NC
5	GPIO	NC	NC	NC	NC
6	VNC/GPIO	GPIO	GPIO	GPIO3	NC
7	GPIO/VDD	PP	PP	PP	PP
8	VDD	VDD	NC	VHIO	VDD
9	GND	GND	NC	NC	GND
10	VNC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
13	VNC/GPIO	NC	NC	GPIO4	NC
14	VDD	NC/VDD	NC	NC	VDD
15	NC	NC	NC	NC	NC
16	GND	NC/GND	NC	GND	GND
17	SPI_RST#	RST#	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	PIRQ/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI/GPIO6	MOSI
22	VDD	VDD	VPS	VHIO	VDD
23	GND	GND	NC	GND	GND
24	MISO	MISO	NC	MISO	MISO
25	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC
29	VNC/GPIO	NC	NC	SDA/GPIO0	NC
30	VNC/GPIO	NC	NC	SCL/GPIO1	NC
31	VNC	GND	NC	NC	NC
32	GND	NC	NC	NC	GND

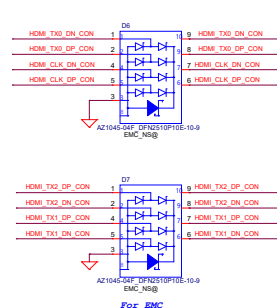
Pin No	TCG PTP Spec (v38)	Infinion SLB9670VQ2.0 FW 7.61	ST Micro ST3TH1PH2E32AHB4	Nuvoton NPCT750LABYX	NATIONZ Z32H333TC
1	VDD	NC/VDD	NC	VSB	VDD
2	GND	GND	GND	NC	GND
3	GPIO	NC	NC	NC	NC
4	GPIO	NC	NC	PP/GPIO6	NC
5	GPIO	NC	NC	NC	NC
6	VNC/GPIO	GPIO	GPIO	GPIO3	NC
7	GPIO/VDD	PP	PP	PP	PP
8	VDD	VDD	NC	VHIO	VDD
9	GND	GND	NC	NC	GND
10	VNC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
13	VNC/GPIO	NC	NC	GPIO4	NC
14	VDD	NC/VDD	NC	NC	VDD
15	NC	NC	NC	NC	NC
16	GND	NC/GND	NC	GND	GND
17	SPI_RST#	RST#	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	PIRQ/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI/GPIO6	MOSI
22	VDD	VDD	VPS	VHIO	VDD
23	GND	GND	NC	GND	GND
24	MISO	MISO	NC	MISO	MISO
25	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC
29	VNC/GPIO	NC	NC	SDA/GPIO0	NC
30	VNC/GPIO	NC	NC	SCL/GPIO1	NC
31	VNC	NC	NC	NC	NC
32	GND	GND	NC	NC	GND

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EMI-request






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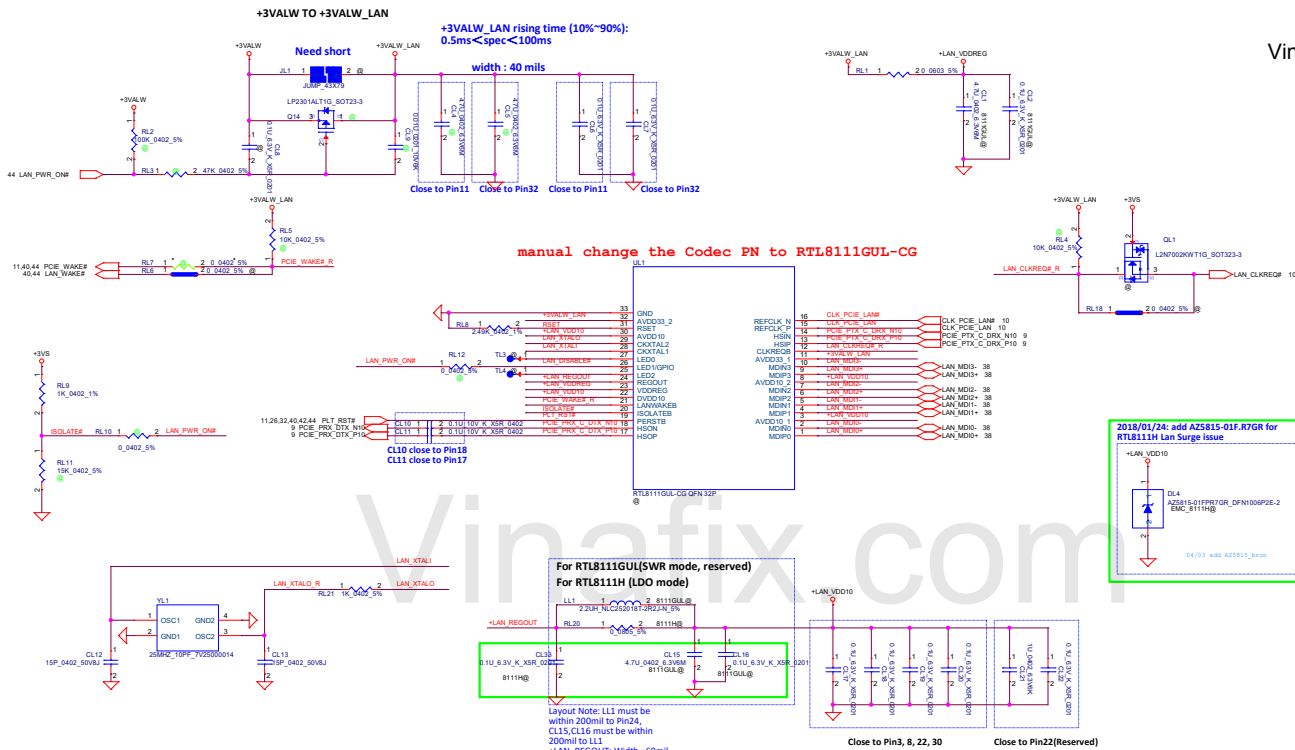
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Issued Date		Deciphered Date		Blank	
2019/07/20		2020/07/20		Blank	
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Size				Document Number	
C				GS55C	
Date				Wednesday, November 20, 2019 18:00	
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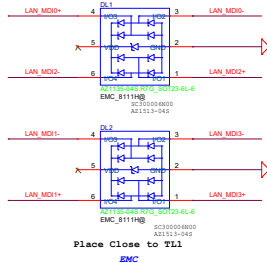
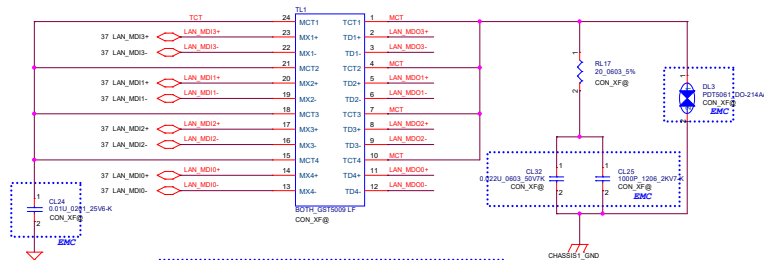


Rev
0.1

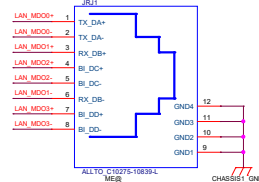
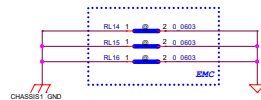
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Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		HALL Sensor	
2019/07/20		2020/07/20			
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Size				Document Number	
G855C				Rev 0.1	
Date				Wednesday, November 20, 2019 18:00	
Sheet				38 of 61	



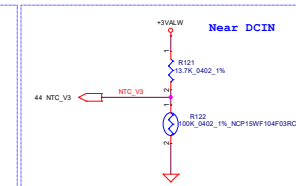
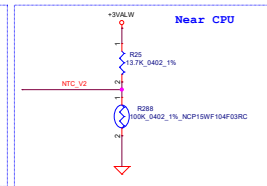
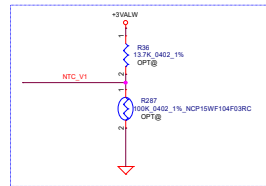
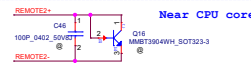
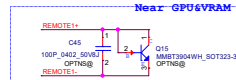
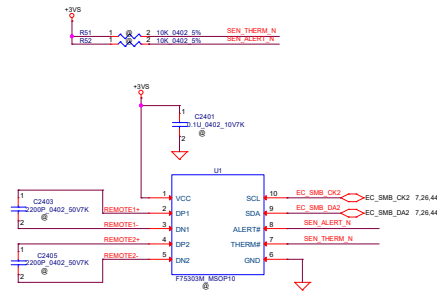


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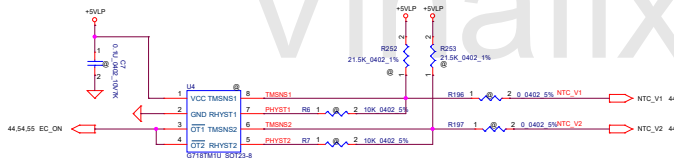


SMSC thermal sensor placed near DIMM

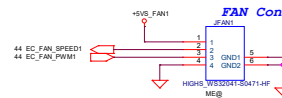
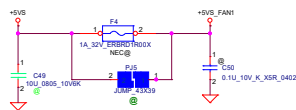
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYSZ=(RSET*RTML) / (3*RTML-RSET)
56+/-30C

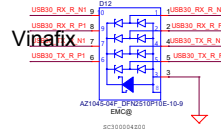
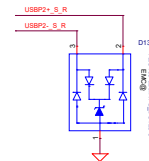
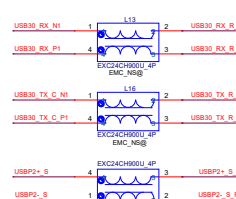
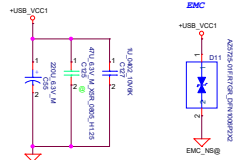
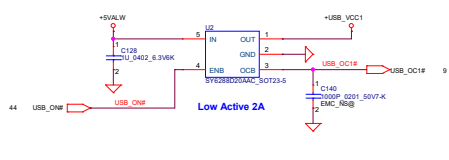


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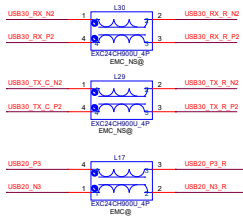
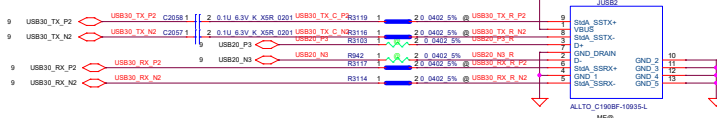
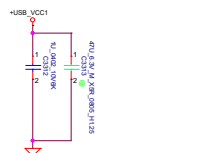
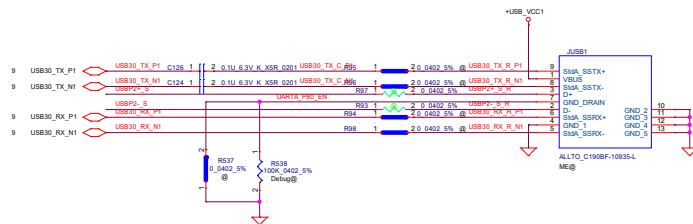
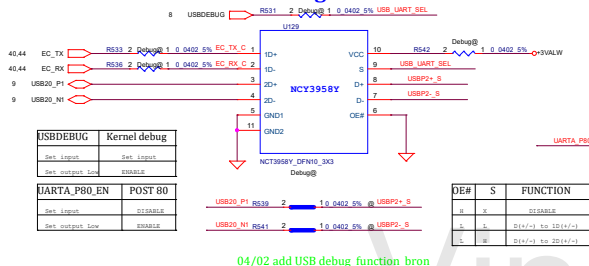
Vinafix

Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		Thermal sensor/FAN CONN	
2019/07/20		2020/07/20		LCFC	
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Size	Document Number		G855C		
Date	Wednesday, November 20, 2019 18:00		Sheet	39	of 61

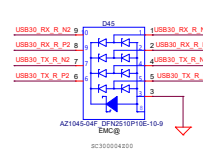
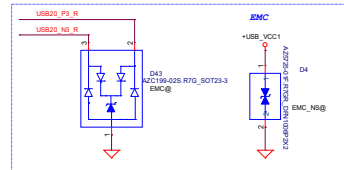
LEFT SIDE USB3.0 PORT x2



For USB Debug Function

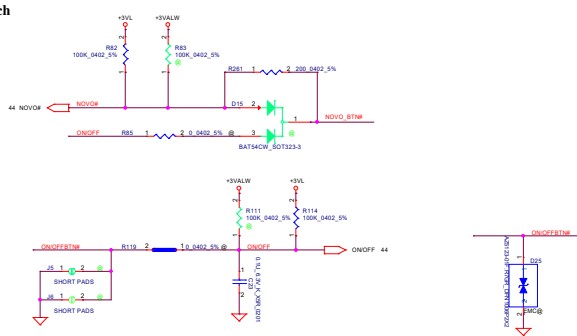


FOR ESD Close to Connector

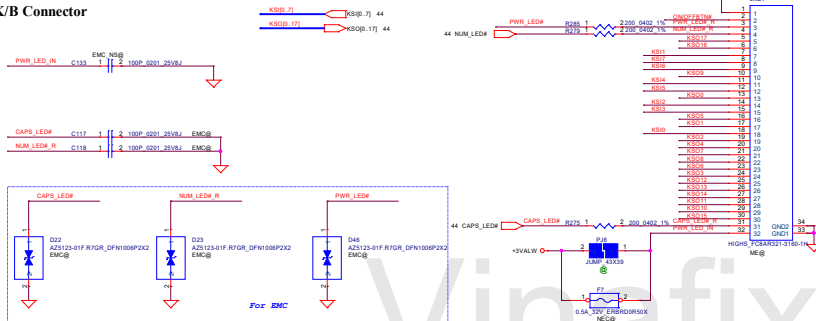


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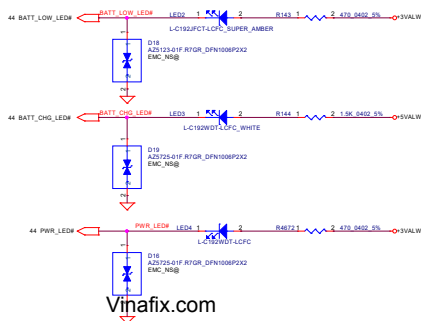
ON/OFF switch



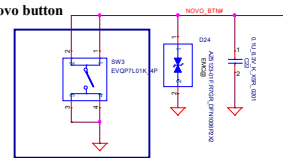
K/B Connector



Finger Print Connector

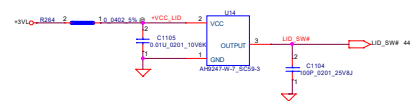


Novo button

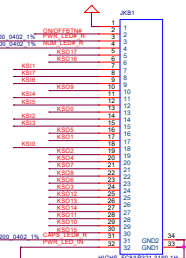


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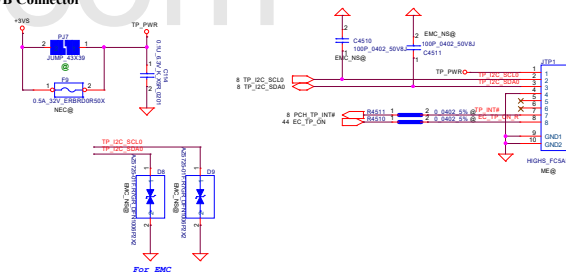
LID switch



KB Backlight Connector



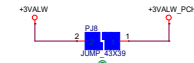
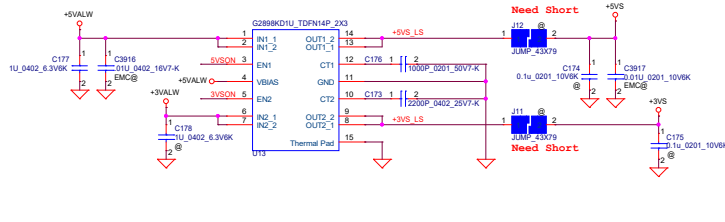
TP/B Connector



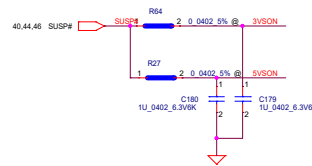
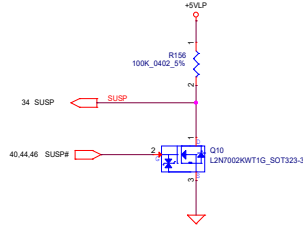
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

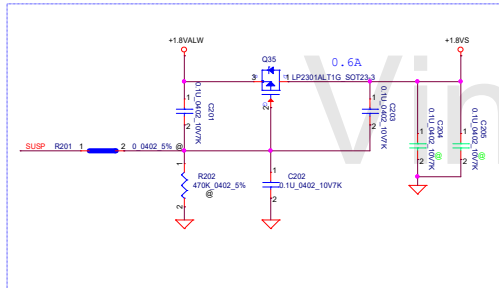
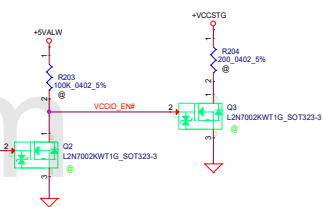
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



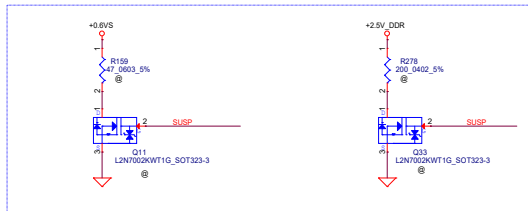
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Reserve for VccSTG discharge



For DisCharge



08/29: Need double check enable signal and the resistance

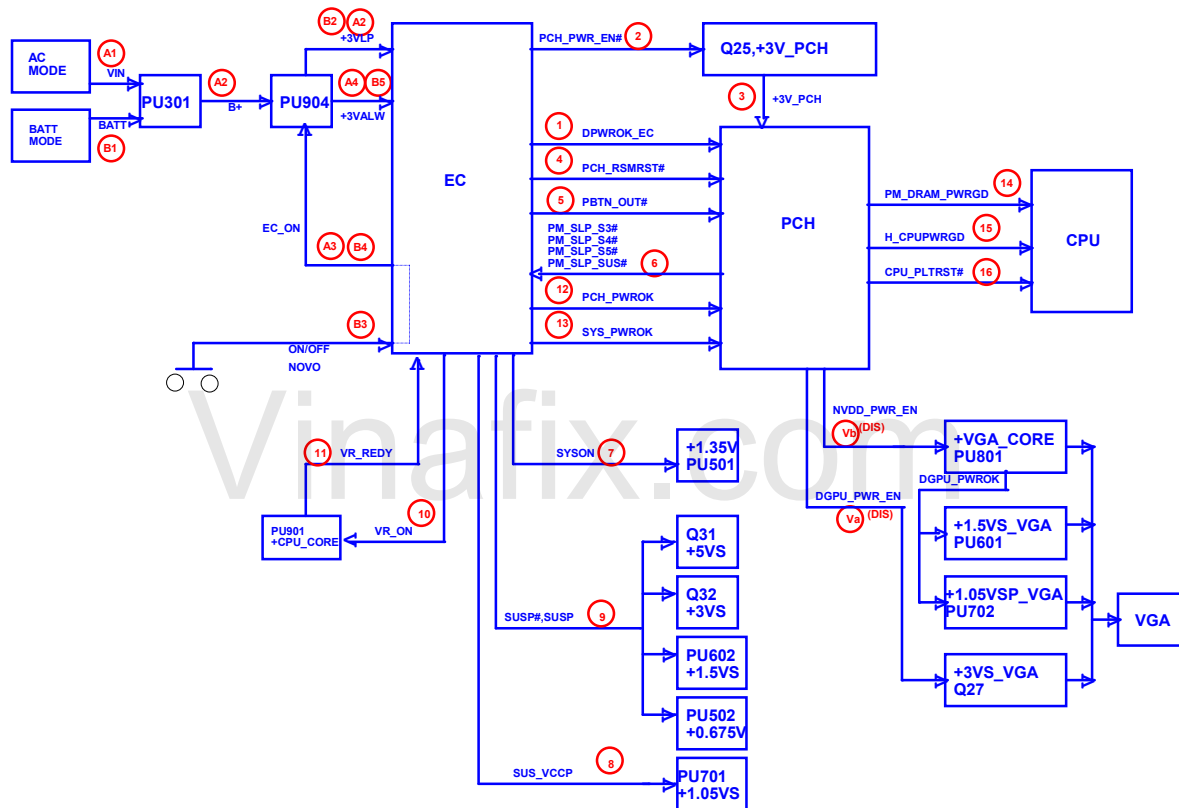
12.1.4 VccSTG Rail Discharge Requirements

As long as VccST and VccSTG are power gated separately, the following requirements are critical to prevent system failure on Whiskey Lake:

1. VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal $R_{\text{discharge}} \leq 300\Omega$ to GND. The discharge circuit should be activated when the VccSTG load switch is disabled.
2. If VccST/VccPLL has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal $R_{\text{discharge}} \leq VccST/VccPLL R_{\text{discharge}}$.
3. The total capacitance on VccSTG \leq total capacitance on VccST/VccPLL.

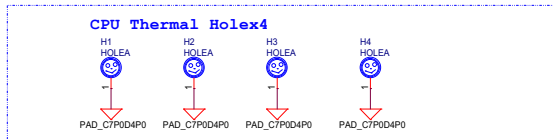
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2019/07/20		2020/07/20		Size	
				Document Number	
				GS55C	
				Date	
				Wednesday, November 20, 2019	
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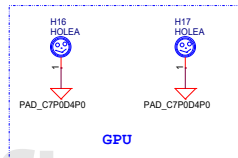
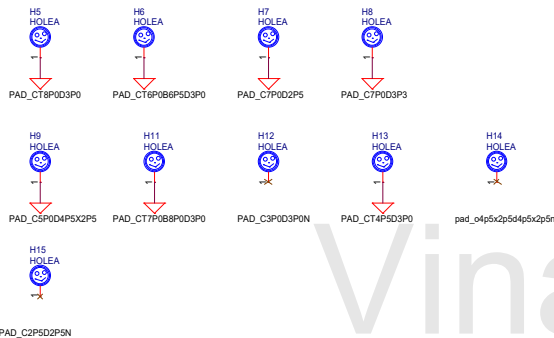
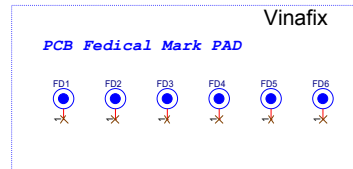


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Close to RJ45

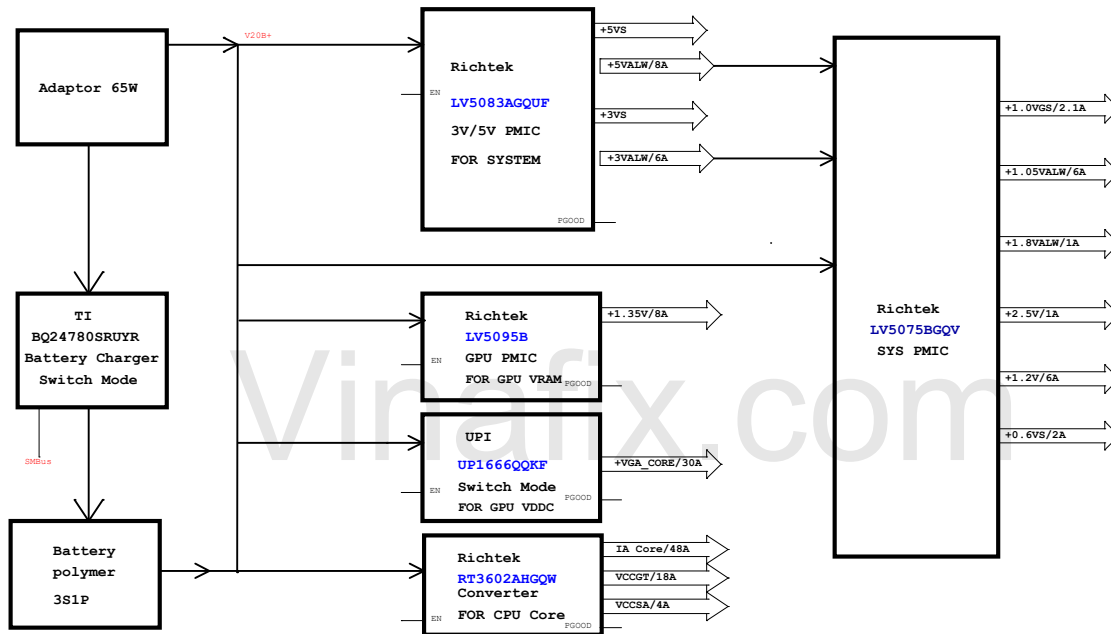


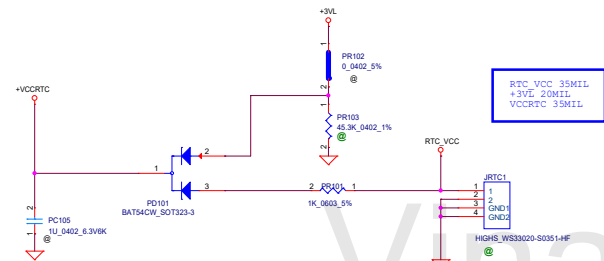
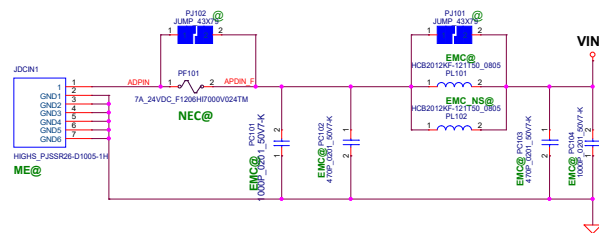
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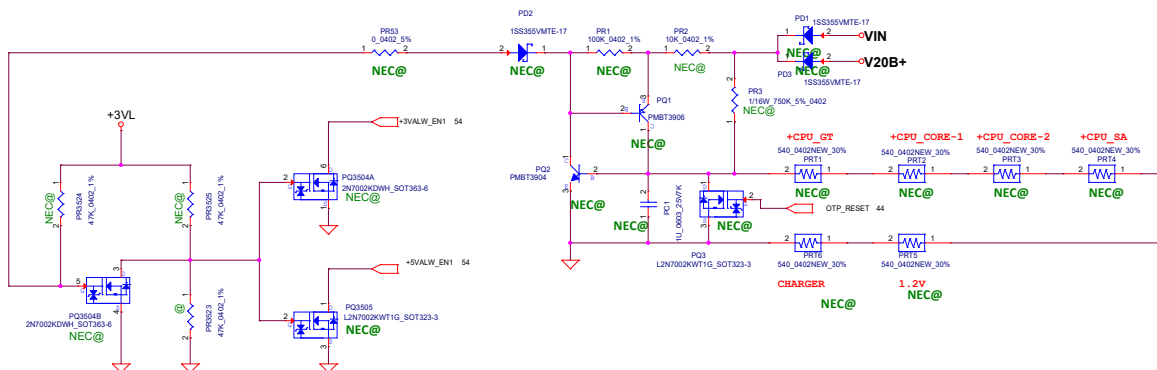
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Date	Wednesday, November 20, 2019	Sheet	49 of 61

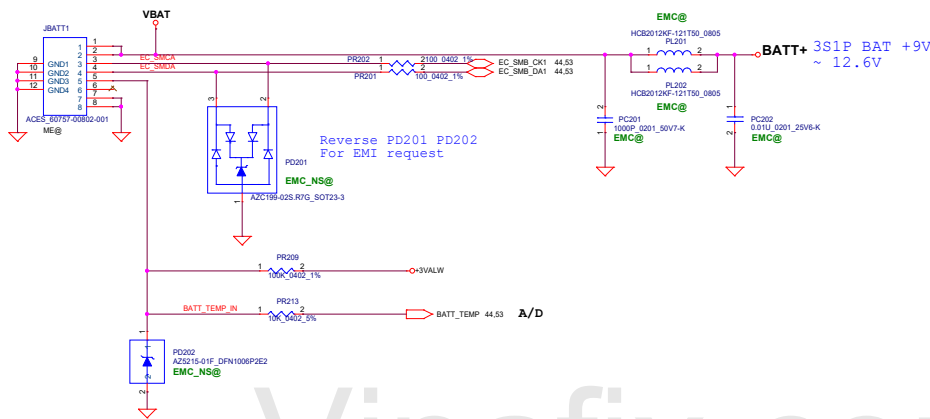




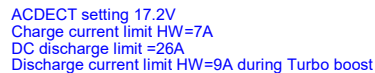


OTP



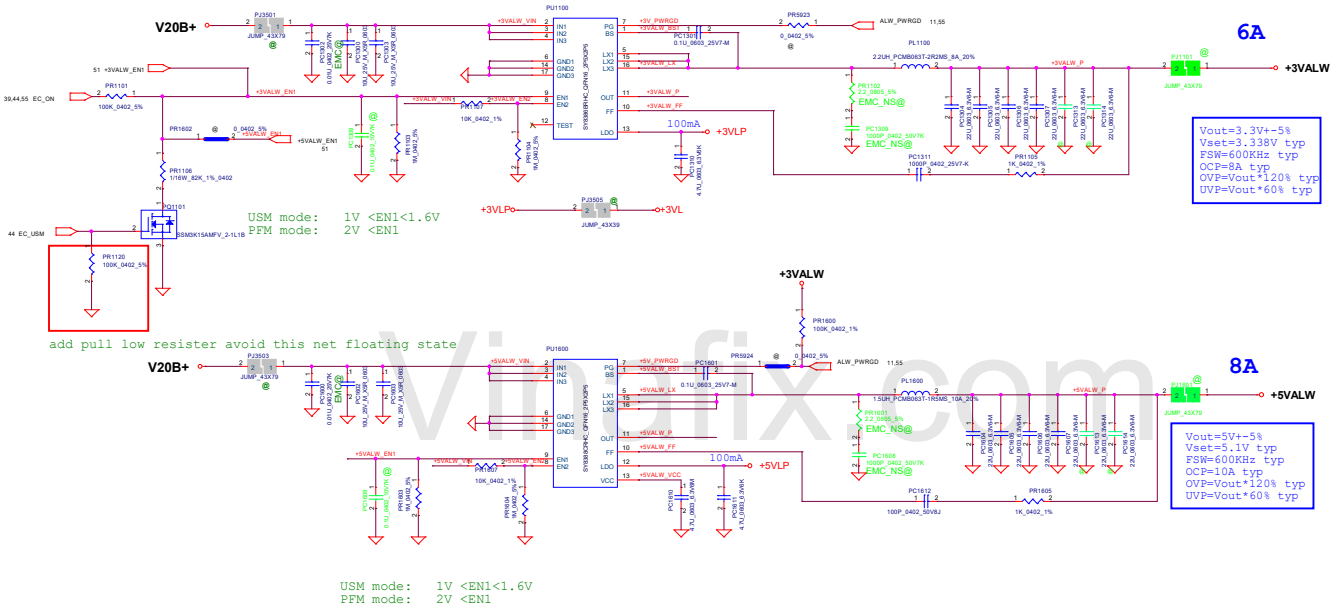


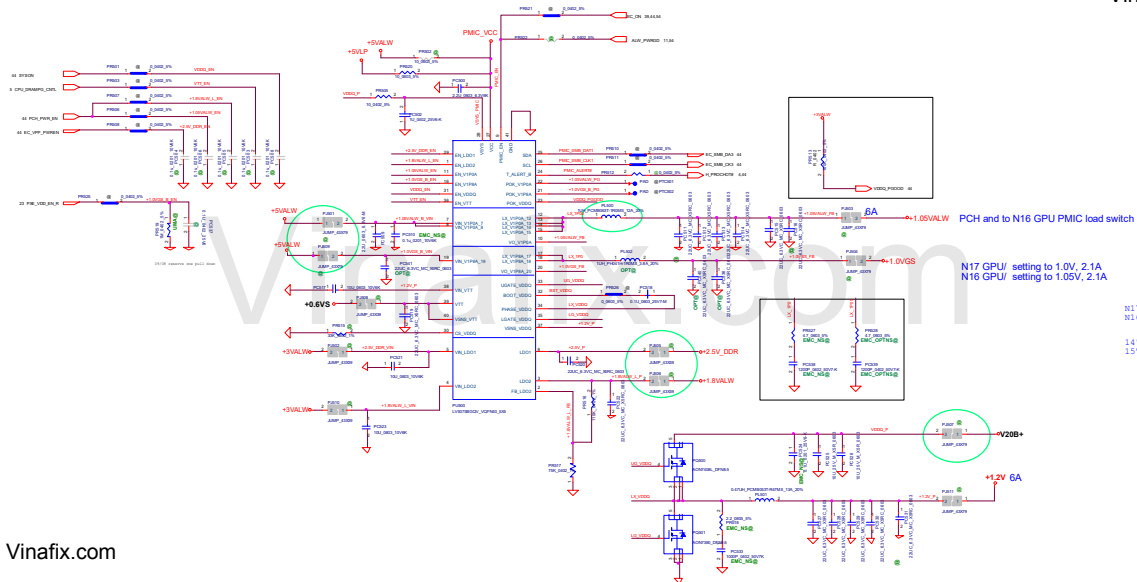
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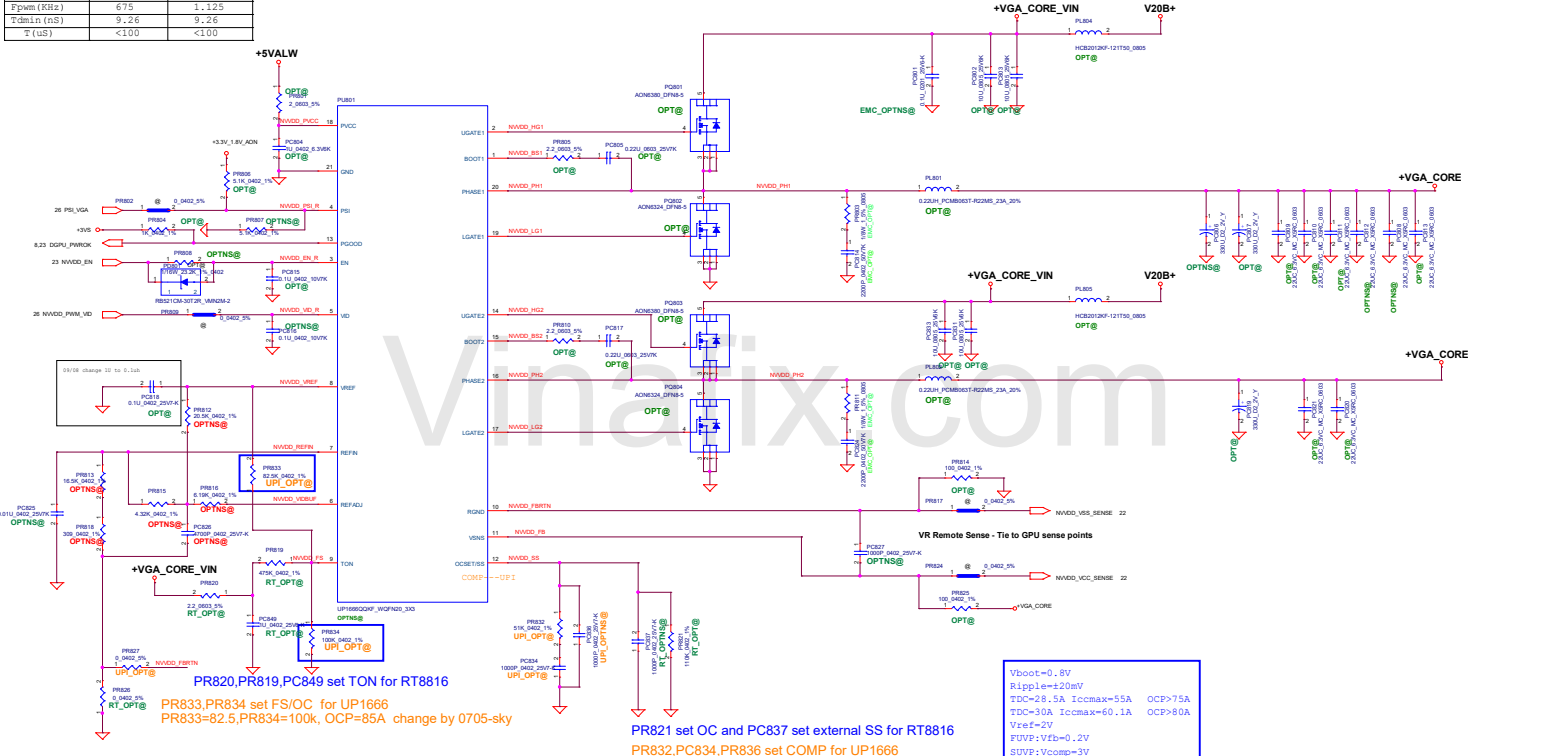




PWM-VID Specification			
	N17 Config	N16 Config B	
Vmin (V)	0.3	0.6	
Vmax (V)	1.3	1.2	
Vboot (V)	0.8	0.9	
Vstep (mV)	6.25	6.25	
N (level)	160	96	
Fpwm (KHz)	675	1.125	
Tdmin (ns)	9.24	9.24	
T (us)	<100	<100	

RT816 PBI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM

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PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

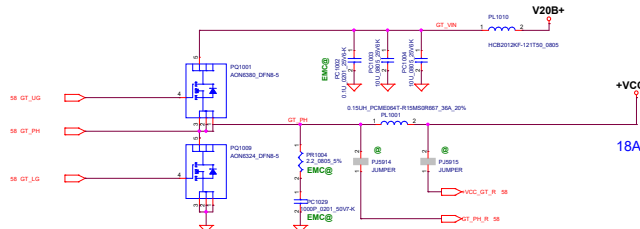
Component	Value	N17	N16
R1 (Ω)	PR816	6.19	20
R2 (KΩ)	PR812	20.5	20
R3 (KΩ)	PR815	4.32	2
R4 (KΩ)	PR813	16.5	1.8
R5 (KΩ)	PR818	0.309	0
C (nF)	PC826	4.7	2.7

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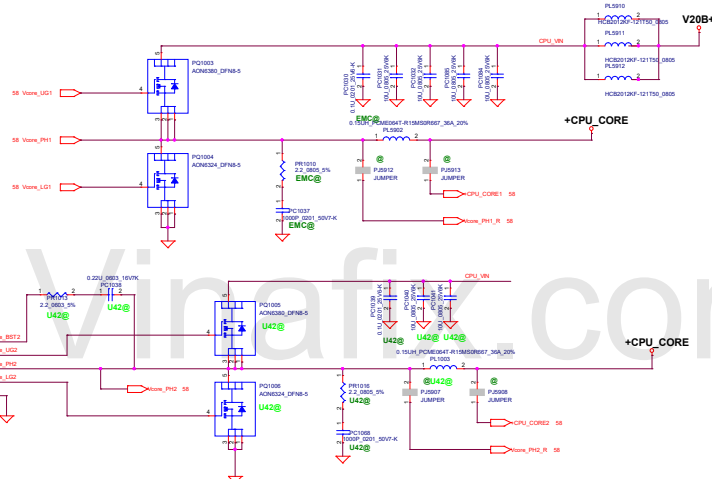
UPL_OPT@ : for UP1666
RT_OPT@ : for RT816A

Vboot=0.8V
Ripple=420mV
TDC=28.5A Iccmax=55A OCP=75A
TDC=30A Iccmax=60.1A OCP=80A
Vref=2V
FVFP:Vfb=0.2V
SUVP:Vcomp=3V
OVP:Vfb=2V
Fsw=320KHz



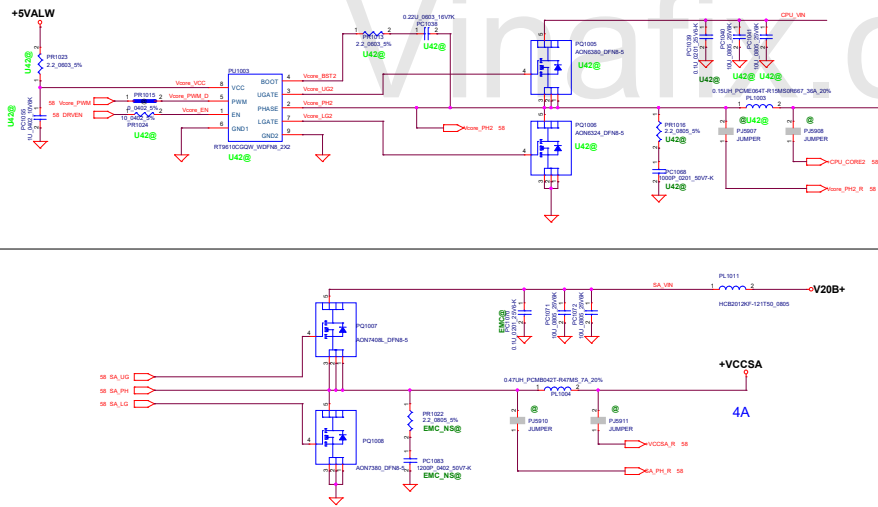


Vboot=0V Loadline=3.1mΩ
 Ripple=+30mV/-10mV (0A~0.5A)
 Ripple=+10mV (0.5A~TDC)
 Ripple=+15mV (TDC-Iccmax)
 TDC=18A Iccmax=31A OCP=37A
 OVP=VID+370mV-VID+430mV
 Max Overshoot:70mV/10us
 UVF=VID-370mV-VID-225mV
 Fsw=550Khz



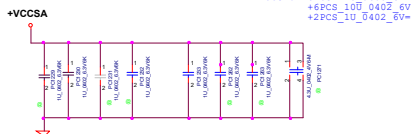
U22 :21A
 U42: 48A

Vboot=0V Loadline=1.8mΩ
 Ripple=+30mV/-10mV (0A~0.5A)
 Ripple=+10mV (0.5A~TDC)
 Ripple=+15mV (TDC-Iccmax)
 TDC=21A/48A Iccmax=32A/70A
 OCP=37A / 74A
 Max Overshoot:70mV/10us
 OVE=VID+370mV-VID+430mV
 UVF=VID-370mV-VID-225mV
 Fsw=550Khz



Vboot=0V Loadline=10.3Ω
 Ripple=+30mV/-10mV (0A~0.5A)
 Ripple=+10mV (0.5A~TDC)
 Ripple=+15mV (TDC-Iccmax)
 TDC=4A Iccmax=4.5A OCP=7A
 Max Overshoot:70mV/10us
 OVP=VID+370mV-VID+430mV
 UVF=VID-370mV-VID-225mV
 Fsw=550Khz

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